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Semiconductor devices - Mechanical and climatic test methods - Part 41: Standard reliability testing methods of non-volatile memory devices

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Part 41: Standard reliability testing methods of non-volatile
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(IEC 60749-41:2020)

Dispositifs à semiconducteurs - Méthodes d'essais
mécaniques et climatiques - Partie 41: Méthodes d'essai
normalisées pour la fiabilité des dispositifs à mémoire non
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(IEC 60749-41:2020)

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Prüfverfahren - Teil 41: Standardisierte Prüfverfahren für
die Zuverlässigkeit von nichtflüchtigen Speicher-
Bauelementen
(IEC 60749-41:2020)

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EN IEC 60749-41:2020 (E)**European foreword**

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<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60749-6	-	Semiconductor devices - Mechanical and climatic test methods - Part 6: Storage at high temperature	EN 60749-6	-
IEC 60749-23	-	Semiconductor devices - Mechanical and climatic test methods - Part 23: High temperature operating life	EN 60749-23	-
JESD47	-	Stress-Test-Driven Qualification of Integrated Circuits	-	-
JESD94	-	Application Specific Qualification Using Knowledge Based Test Methodology	-	-



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INTERNATIONAL STANDARD

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**Semiconductor devices – Mechanical and climatic test methods –
Part 41: Standard reliability testing methods of non-volatile memory devices**

**Dispositifs à semiconducteurs – Méthodes d'essais mécaniques
et climatiques –
Partie 41: Méthodes d'essai normalisées pour la fiabilité des dispositifs
à mémoire non volatile**





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à mémoire non volatile**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

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FDIS	Report on voting
47/2631/FDIS	47/2643/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

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INTRODUCTION

The stress tests described in this part of IEC 60749 are intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention).

The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. The data retention stress can be used as a proxy to replace the high temperature storage life test when the temperature and time meet or exceed qualification requirements. Cross-temperature testing for writing and reading across the data sheet temperature range can be considered when there are demonstrated sensitivities for programming at low and reading at high temperatures or vice versa. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) can be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

1 Scope

This part of IEC 60749 specifies the procedural requirements for performing valid endurance, retention and cross-temperature tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or are developed using knowledge-based methods such as in JESD94.

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