

<b>STN</b>	<b>Skúšobné metódy na elektrotechnické materiály, dosky s plošnými spojmi a iné spájacie štruktúry a zostavy</b> <b>Časť 5-501: Všeobecné skúšobné metódy na materiály a zostavy</b> <b>Skúšanie spájkovacích tavidiel na odolnosť povrchovej izolácie (SIR)</b>	<b>STN EN IEC 61189-5-501</b>  34 6513
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Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-501: General test methods for materials and assemblies - Surface insulation resistance (SIR) testing of solder fluxes

Táto norma obsahuje anglickú verziu európskej normy.  
This standard includes the English version of the European Standard.

Táto norma bola oznámená vo Vestníku ÚNMS SR č. 06/21

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Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-501: General test methods for materials and assemblies - Surface insulation resistance (SIR) testing of solder fluxes  
(IEC 61189-5-501:2021)

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles - Partie 5-501: Méthodes d'essai générales pour les matériaux et les ensembles - Essais de résistance d'isolement en surface (RIS) des flux de brasage  
(IEC 61189-5-501:2021)

Prüfverfahren für Elektromaterialien, Leiterplatten und andere Verbindungsstrukturen und Baugruppen - Teil 5-501: Allgemeine Prüfverfahren für Materialien und Baugruppen - Prüfung des Oberflächenisolationswiderstands (SIR) von Lotflussmitteln  
(IEC 61189-5-501:2021)

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Comité Européen de Normalisation Electrotechnique  
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**EN IEC 61189-5-501:2021 (E)****European foreword**

The text of document 91/1645/CDV, future edition 1 of IEC 61189-5-501, prepared by IEC/TC 91 “Electronics assembly technology” was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 61189-5-501:2021.

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 61189-1	NOTE	Harmonized as EN 61189-1
IEC 61189-3	NOTE	Harmonized as EN 61189-3
IEC 61190-1-1	NOTE	Harmonized as EN 61190-1-1
IEC 61190-1-2:2014	NOTE	Harmonized as EN 61190-1-2:2014 (not modified)
IEC 61191-1	NOTE	Harmonized as EN IEC 61191-1
ISO 9455-1	NOTE	Harmonized as EN 29455-1
ISO 9455-2	NOTE	Harmonized as EN ISO 9455-2
ISO 9455-17	NOTE	Harmonized as EN ISO 9455-17

## Annex ZA (normative)

### Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: [www.cenelec.eu](http://www.cenelec.eu).

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60068-1	2013	Environmental testing - Part 1: General and guidance	EN 60068-1	2014
IEC 60068-2-58	-	Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)	EN 60068-2-58	-
IEC 60068-2-67	-	Environmental testing - Part 2-67: Tests - Test Cy: Damp heat, steady-state, accelerated test primarily intended for components	EN 60068-2-67	-
IEC 60068-2-78	-	Environmental testing - Part 2-78: Tests - Test Cab: Damp heat, steady-state	EN 60068-2-78	-
IEC 60194-2	-	Printed boards design, manufacture and assembly - Vocabulary - Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies	-	-
IEC 61189-5-504	-	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-504: General test methods for materials and assemblies - Process ionic contamination testing (PICT)	EN IEC 61189-5-504	-

**EN IEC 61189-5-501:2021 (E)**

IEC/TR 61189-5-506	-	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5–506: General test methods for materials and assemblies - An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501	-
IEC 61190-1-3	-	Attachment materials for electronic assembly - Part 1–3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solder for electronic soldering applications	EN IEC 61190-1-3 -
IEC 61249-2-7	-	Materials for printed boards and other interconnecting structures - Part 2–7: Reinforced base materials clad and unclad - Epoxide woven E-glass laminated sheet of defined flammability (vertical burning test), copper-clad	EN 61249-2-7 -



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Edition 1.0 2021-01

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE



**Test methods for electrical materials, printed boards and other interconnection structures and assemblies –**

**Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes**

**Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –**

**Partie 5-501: Méthodes d'essai générales pour les matériaux et les ensembles – Essais de résistance d'isolement en surface (RIS) des flux de brasage**

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IEC 61189-5-501

Edition 1.0 2021-01

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE



**Test methods for electrical materials, printed boards and other interconnection structures and assemblies –  
Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes**

**Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –  
Partie 5-501: Méthodes d'essai générales pour les matériaux et les ensembles – Essais de résistance d'isolement en surface (RIS) des flux de brasage**

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## CONTENTS

FOREWORD.....	4
1 Scope.....	6
2 Normative references .....	6
3 Terms and definitions .....	7
4 Equipment/Apparatus .....	7
4.1 Measurement instrument.....	7
4.2 Resistor verification coupon .....	8
4.3 Damp heat chamber.....	8
4.4 Additional apparatus .....	9
4.4.1 Ionic contamination test system .....	9
4.4.2 Drying oven .....	9
4.4.3 Camera .....	9
4.4.4 Backlight panel .....	9
5 Test coupons.....	9
5.1 General.....	9
5.2 IEC TB144 (IPC B53) test coupon .....	9
5.3 Laminate.....	10
5.4 Coupons for testing.....	10
5.5 Chamber controls.....	10
5.6 Blank process controls .....	11
5.7 Test conditions .....	11
5.7.1 Fluxes not intended for cleaning .....	11
5.7.2 Fluxes intended for cleaning .....	11
5.8 Test duration.....	11
5.9 Test voltage .....	11
5.10 Connecting the test coupons .....	11
5.10.1 General .....	11
5.10.2 Connector/test rack .....	11
5.10.3 Direct wiring .....	12
5.11 Cable connection .....	12
5.12 Coupon orientation in the chamber .....	12
6 Coupon preparation .....	13
6.1 General.....	13
6.2 Coupon cleaning.....	13
6.3 Identification .....	13
6.4 Inspection .....	13
6.5 Storage.....	13
6.6 No clean fluxes .....	14
6.7 Cleanable type fluxes.....	14
6.8 Solder paste coupons .....	14
6.8.1 Coupon preparation .....	14
6.8.2 Cleaning of coupons .....	15
6.9 Preparation of coupons for chamber .....	15
7 Test procedure .....	15
8 Measurements.....	15
9 Evaluation .....	15

10 Reporting.....	16
Annex A (informative) General advice for testing .....	17
A.1 Test coupons .....	17
A.2 Test coupon development .....	17
A.3 Sampling.....	17
A.3.1 General .....	17
A.3.2 Coupon count .....	17
A.3.3 Sample sizes .....	17
A.3.4 Characterising materials .....	17
A.3.5 Characterising process(es).....	17
A.3.6 Derived unit of SIR .....	17
A.3.7 Set-up parameters .....	18
A.4 Humidity .....	18
A.5 Voltage .....	18
Bibliography.....	19
Figure 1 – SIR pattern .....	6
Figure 2 – Example of a resistor verification coupon .....	8
Figure 3 – IPC B53 Surface insulation resistance pattern.....	10
Figure 4 – Connector arrangement.....	12
Figure 5 – Specimen orientation in test chamber.....	12
Figure 6 – Coupon orientation in test chamber .....	13
Table 1 – Coupons for surface insulation resistance (SIR) testing.....	14

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS  
AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –****Part 5-501: General test methods for materials and assemblies –  
Surface insulation resistance (SIR) testing of solder fluxes**

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The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1645/CDV	91/1672/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at [www.iec.ch/members\\_experts/refdocs](http://www.iec.ch/members_experts/refdocs). The main document types developed by IEC are described in greater detail at [www.iec.ch/standardsdev/publications](http://www.iec.ch/standardsdev/publications).

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# TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

## Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes

### 1 Scope

This part of IEC 61189 is used to quantify the deleterious effects of flux residues on surface insulation resistance (SIR) in the presence of moisture.

Interdigitated comb patterns comprising long parallel electrodes on an IPC B53 standardized test coupon are used for the evaluation. Coupons are conditioned and measurements taken at a high temperature and humidity. The electrodes are electrically biased during conditioning to facilitate electrochemical reactions, as shown in Figure 1 and Figure 3.

Reference can be made to IEC TR 61189-5-506, which examines different geometry comb patterns: 400  $\mu\text{m}$  x 500  $\mu\text{m}$ ; 400  $\mu\text{m}$  x 200  $\mu\text{m}$ ; and 318  $\mu\text{m}$  x 318  $\mu\text{m}$ .

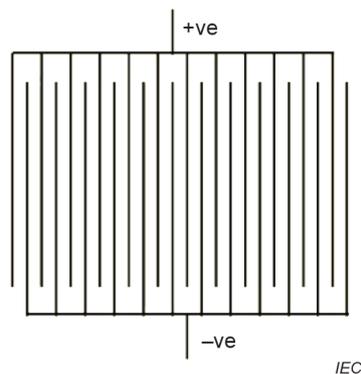


Figure 1 – SIR pattern

Specifically, this method is designed to simultaneously assess:

- leakage current caused by ionized water films and electrochemical degradation of test vehicle, (corrosion, dendritic growth);
- provide metrics that can appropriately be used for binary classification (e.g. go/no go; pass/fail);
- compare, rank or characterize materials and processes.

This test is carried out at high humidity and heat conditions.

### 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1:2013, *Environmental testing – Part 1: General and guidance*

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60068-2-67, *Environmental testing – Part 2-67: Tests – Test Cy: Damp heat, steady state, accelerated test primarily intended for components*

IEC 60068-2-78, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

IEC 61189-5-504, *Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 5-504: General test methods for materials and assemblies – Process ionic contamination testing (PICT)*

IEC TR 61189-5-506, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-506: General test methods for materials and assemblies – An intercomparison evaluation to implement the use of fine pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501*

IEC 61190-1-3, *Attachment materials for electronic assembly – Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solder for electronic soldering applications*

IEC 61249-2-7, *Materials for printed boards and other interconnecting structures – Part 2-7: Reinforced base materials clad and unclad – Epoxide woven E-glass laminated sheet of defined flammability (vertical burning test), copper-clad*

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