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Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices

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**Dynamic on-resistance test method guidelines for GaN HEMT
based power conversion devices
(IEC 63373:2022)**

Lignes directrices pour les méthodes d'essai de résistance
dynamique à l'état passant des dispositifs de conversion de
puissance fondés sur les HEMT en GaN
(IEC 63373:2022)

Richtlinien für Prüfverfahren des dynamischen
Einschaltwiderstandes bei GaN-HEMT-Leistungswandlern
(IEC 63373:2022)

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Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices

Lignes directrices pour les méthodes d'essai de résistance dynamique à l'état passant des dispositifs de conversion de puissance fondés sur les HEMT en GaN

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES
FOR GaN HEMT BASED POWER CONVERSION DEVICES**

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

¹ Numbers in square brackets refer to the Bibliography.

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INTRODUCTION

This document is intended for use in the GaN power semiconductor and related power electronic industries, and provides guidelines for measuring the dynamic ON-resistance of GaN power devices.

Gallium Nitride (GaN) lateral power High Electron Mobility Transistor (HEMT) conducts through a two-dimensional electron gas (2DEG) in ON-state operation. Due to the various stress conditions that the device encounters during power electronic switching applications, some charge could get trapped in specific regions of the transistor structure. The trapped electrons cause an increased ON-resistance when operated in a switching environment. This phenomenon is known as current collapse and the ON-resistance at switching operation is called dynamic ON-resistance in order to distinguish from DC ON-resistance. Increased dynamic ON-resistance translates to higher power loss, thereby reducing overall system efficiency. Not verifying the dynamic ON-resistance characteristic can put GaN device reliability at risk [2].

The test methods provided in this document can be used as a guideline for measuring dynamic ON-resistance of GaN power device, focused on lateral HEMT technologies. These three test methods can be applied for datasheet, process control, technology development, final tests and other usage. Parasitic effects impact high precision measurements and wafer level tests can minimize parasitic effects. Additionally, self-heating can impact the package level tests depending upon the package thermal characteristics.

DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES

1 Scope

In general, dynamic ON-resistance testing is a measure of charge trapping phenomena in GaN power transistors. This publication provides guidelines for testing dynamic ON-resistance of GaN lateral power transistor solutions. The test methods can be applied to the following:

- a) GaN enhancement and depletion-mode discrete power devices [3];
- b) GaN integrated power solutions;
- c) the above in wafer and package levels.

The prescribed test methods can be used for device characterization, production testing, reliability evaluations and application assessments of GaN power conversion devices. This document is not intended to cover the underlying mechanisms of dynamic ON-resistance and its symbolic representation for product specifications.

2 Normative references

There are no normative references in this document.

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