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Device embedding assembly technology - Part 2-603: Guideline for stacked electronic module - Test method of intra-module electrical connectivity

Táto norma obsahuje anglickú verziu európskej normy.

This standard includes the English version of the European Standard.

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EN IEC 62878-2-603

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English Version

**Device embedding assembly technology - Part 2-603: Guideline
for stacked electronic module - Test method of intra-module
electrical connectivity
(IEC 62878-2-603:2025)**

Techniques d'assemblage avec appareil(s) intégré(s) -
Partie 2-603: Lignes directrices pour un empilement de
modules électroniques - Méthode d'essai de la connectivité
électrique entre modules
(IEC 62878-2-603:2025)

Technologie zur Einbettung von Bauelementen - Teil 2-603:
Leitfaden für gestapelte elektronische Module -
Prüfverfahren für die elektrische Konnektivität innerhalb des
Moduls
(IEC 62878-2-603:2025)

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EN IEC 62878-2-603:2025 (E)**European foreword**

The text of document 91/1999/FDIS, future edition 1 of IEC 62878-2-603, prepared by TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62878-2-603:2025.

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Annex ZA

(normative)

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<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60194-2	-	Printed boards design, manufacture and assembly - Vocabulary - Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies	-	-



IEC 62878-2-603

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INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Device embedding assembly technology –
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**Techniques d'assemblage avec appareil(s) intégré(s) –
Partie 2-603: Lignes directrices pour un empilement de modules électroniques –
Méthode d'essai de la connectivité électrique entre modules**

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CONTENTS

FOREWORD.....	3
INTRODUCTION.....	5
1 Scope.....	6
2 Normative references	6
3 Terms, definitions and abbreviated terms	6
3.1 Terms definitions	6
3.2 Abbreviated terms.....	6
4 General	7
5 Test specimen	8
5.1 General.....	8
5.2 Preparation of test specimen.....	8
6 Test apparatus	9
7 Test method and test procedure	10
7.1 General.....	10
7.2 Example of a test procedure	10
Annex A (informative) Representatives of bidirectional serial bus communication interface	12
Bibliography.....	13
 Figure 1 – SAEM (stackable electronic module)	7
Figure 2 – SDEM (stacked electronic module).....	7
Figure 3 – Inter-module connection and intra-module connection	8
Figure 4 – Image drawing of the test specimen	9
Figure 5 – Test apparatus	10
Figure 6 – Test procedure.....	11
 Table A.1 – Representatives of bidirectional serial communication bus interface	12

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

**Part 2-603: Guideline for stacked electronic module –
Test method of intra-module electrical connectivity**

FOREWORD

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The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1999/FDIS	91/2016/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

INTRODUCTION

High-end servers, network systems, PCs and smart phones have been driving the electronic assembly technologies for the last couple of decades. In order to meet higher demands in computing load from cloud computing and large scale of datacentres with low energy consumption and cost-effective manner, it is important that IoT and edge computing devices achieve greater miniaturization and densification. Stacked electronic module which offers complex and simultaneous integration of various functional modules and specific features is a solution that can meet these demands. The stacked electronic module is produced by means of stacking some stackable electronic modules. The stackable electronic module usually mounts components with area array type package (BGA, LGA, and similar) on the surface and does embed components with wafer-level type package or bare chip into the inner layer to achieve miniaturization and densification. However, from a viewpoint of test and diagnosis the stacked electronic module becomes an invisible, untouchable and undiagnosed structure. Due to its design and construction complexity, it is increasingly critical to test a stacked electronic module with a combination of conventional methods such as external input/output (I/O) terminal or in-circuit test with advanced methods (e.g. boundary scan or bi-directional bus control).

This document is one of a series of guidelines for stacked electronic modules.

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-603: Guideline for stacked electronic module – Test method of intra-module electrical connectivity

1 Scope

This part of IEC 62878 specifies the electrical test method to detect electrical connectivity defects of the stacked electronic module caused by the stacking assembly process to stack some stackable electronic modules. This method is realized to make use of bidirectional serial communication bus interface applied to the stackable electronic modules which are assured as "known good module" (KGM).

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