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**STN**

# Tepelná normalizácia polovodičových puzdier Časť 3: Simulačné modely tepelných obvodov diskrétnych polovodičových puzdier pre prechodovú analýzu

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Thermal standardization on semiconductor packages - Part 3: Thermal circuit simulation models of discrete semiconductor packages for transient analysis

Táto norma obsahuje anglickú verziu európskej normy.
This standard includes the English version of the European Standard.

Táto norma bola oznámená vo Vestníku ÚNMS SR č. 10/25

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EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

**EN IEC 63378-3**

June 2025

ICS 31.080.01

English Version

# Thermal standardization on semiconductor packages - Part 3: Thermal circuit simulation models of discrete semiconductor packages for transient analysis (IEC 63378-3:2025)

Normalisation thermique des boîtiers de semiconducteurs - Partie 3: Modèles de simulation de circuits thermiques de boîtiers de semiconducteurs discrets pour analyse transitoire
(IEC 63378-3:2025)

Thermische Standardisierung von Halbleitergehäusen - Teil 3: Thermische Schaltungssimulationsmodelle von diskreten Halbleitergehäusen für die Transientenanalyse
(IEC 63378-3:2025)

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# European foreword

The text of document 47D/967/CDV, future edition 1 of IEC 63378-3, prepared by SC 47D "Semiconductor devices packaging" of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 63378-3:2025.

The following dates are fixed:

| | | |
|---|---|---|
| • latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement | (dop) | 2026-06-30 |
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IEC 63378-3

Edition 1.0 2025-05

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# NORME INTERNATIONALE

## Thermal standardization on semiconductor packages – Part 3: Thermal circuit simulation models of discrete semiconductor packages for transient analysis

## Normalisation thermique des boîtiers de semiconducteurs – Partie 3: Modèles de simulation de circuits thermiques de boîtiers de semiconducteurs discrets pour analyse transitoire

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# THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

## Part 3: Thermal circuit simulation models of discrete semiconductor packages for transient analysis

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IEC 63378-3 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

| Draft | Report on voting |
|---|---|
| 47D/967/CDV | 47D/979/RVC |

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63378 series, published under the general title *Thermal standardization on semiconductor packages*, can be found on the IEC website.

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- revised.

# THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

# Part 3: Thermal circuit simulation models of discrete semiconductor packages for transient analysis

## 1 Scope

This part of IEC 63378 specifies the thermal circuit network model of discrete (TO-243, TO-252 and TO-263) packages, which is used in the transient analysis of electronic devices to estimate precise junction temperatures without experimental verification.

This model is intended to be made and provided by semiconductor suppliers and to be used by assembly makers of electronic devices.

## 2 Normative references

There are no normative references in this document.