

STN	Tepelná normalizácia polovodičových puzdier Časť 6: Model tepelného odporu a tepelnej kapacity na predikciu prechodnej teploty v prechode a v bodoch merania	STN EN IEC 63378-6 35 8790
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Thermal standardization on semiconductor packages - Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points

Táto norma obsahuje anglickú verziu európskej normy.
This standard includes the English version of the European Standard.

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EUROPEAN STANDARD
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EN IEC 63378-6

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English Version

**Thermal standardization on semiconductor packages - Part 6:
Thermal resistance and capacitance model for transient
temperature prediction at junction and measurement points
(IEC 63378-6:2026)**

Normalisation thermique des boîtiers de semiconducteurs -
Partie 6: Modèle de résistance thermique et de capacité
pour la prédiction de la température transitoire aux points
de jonction et de mesure
(IEC 63378-6:2026)

Thermische Normung an Halbleitergehäusen - Teil 6:
Wärmewiderstandsmodell für die Vorhersage der
vorübergehenden Temperatur an Sperrschicht- und
Messpunkten
(IEC 63378-6:2026)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

EN IEC 63378-6:2026 (E)**European foreword**

The text of document 47D/991/CDV, future edition 1 of IEC 63378-6, prepared by SC 47D "Semiconductor devices packaging" of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 63378-6:2026.

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IEC 63378-6

Edition 1.0 2026-02

INTERNATIONAL STANDARD

**Thermal standardization on semiconductor packages -
Part 6: Thermal resistance and capacitance model for transient temperature
prediction at junction and measurement points**

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**Thermal standardization on semiconductor packages -
Part 6: Thermal resistance and capacitance model for transient
temperature prediction at junction and measurement points**

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The text of this International Standard is based on the following documents:

Draft	Report on voting
47D/991/CDV	47D/998/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

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This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63378 series, published under the general title *Thermal standardization on semiconductor packages*, can be found on the IEC website.

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- reconfirmed,
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- revised.

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INTRODUCTION

The IEC 63378-6 series is composed of the following parts:

- IEC 63378-6-1 [1]^{1,2} defines the model creation method using a datasheet of semiconductor devices.
- IEC 63378-6-2³ defines the model creation method using measurement data of semiconductor devices.

The IEC 63378-6 series includes subjects such as the definition of a new thermal compact model for thermal transient analysis of semiconductor packages, model creation methods, accuracy assessment of these models, etc.

¹ Numbers in square brackets refer to the Bibliography.

² Under preparation. Stage at the time of publication: IEC APUB 63378-6-1:2026.

³ Under development.

1 Scope

This part of IEC 63378 specifies a thermal resistance and capacitance model for semiconductor packages. This model is named the digital transformation using thermal resistance and capacitance (DXRC) model. It predicts transient temperature at junction and measurement points.

This document applies to semiconductor packages such as TO-252, TO-263, and HSOP. It supports single chip packages dissipated heat from single package surface.

2 Normative references

There are no normative references in this document.

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